PROMETHEUS FPGA
DEVELOPMENT BOARDS & MORE

27/02/2017
REV: 1.0

PROMETHEUS

FPGA DEVELOPMENT BOARD
USER MANUAL: REV C (Board)

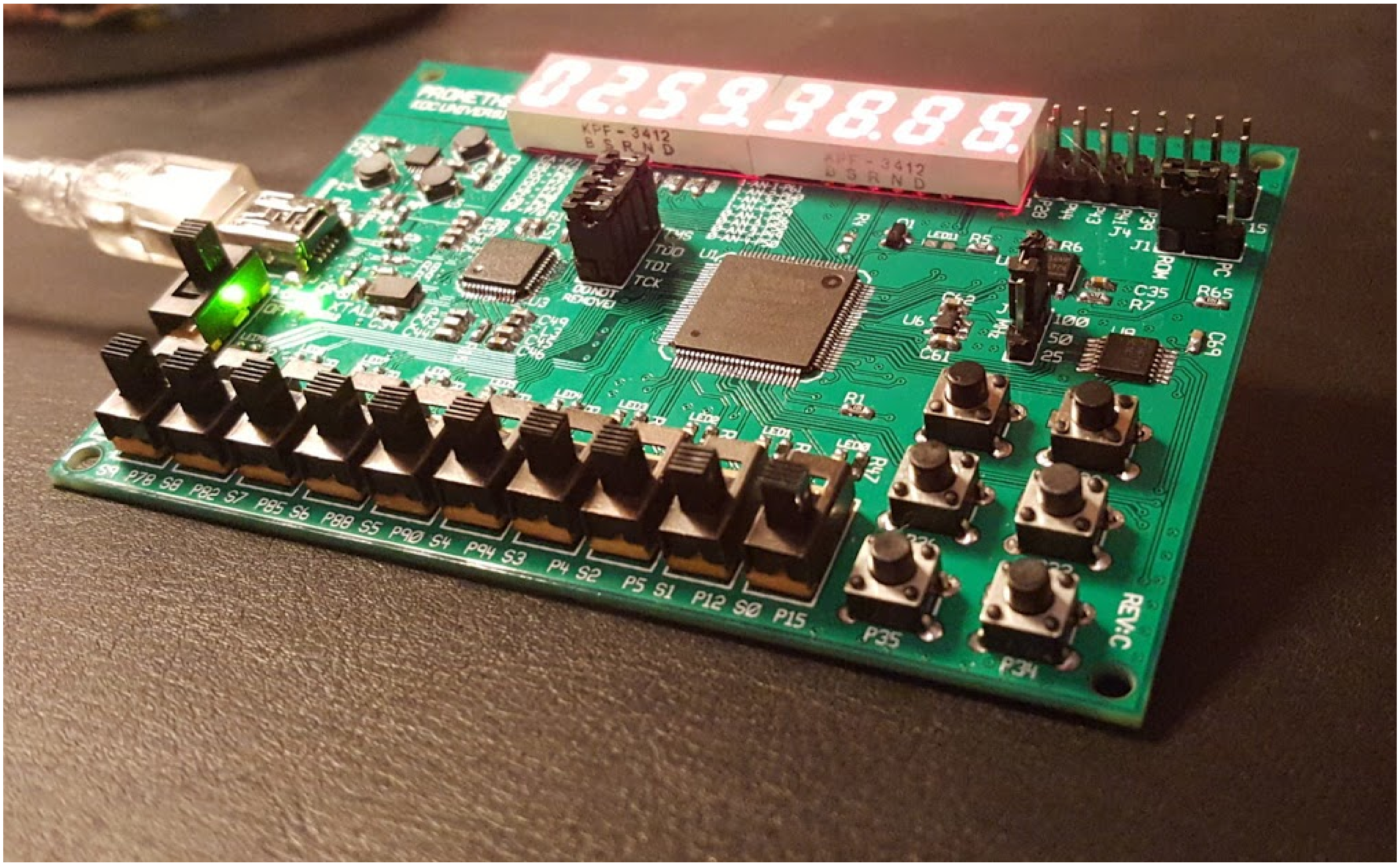
KPF-3412
KPF-3412
TMS
TDO
TDI
TCK
DONOT REMOVE
S9 P78 S8 P82 S7 P85 S6 P88 S5 P9Ø S4 P94 S3 P4 S2 P5 S1 P12 SØ P15
P35
P34
REV:C

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TABLE OF CONTENTS

1. INTRODUCTION

1.1. BLOCK DIAGRAM P 3
1.2. BOARD OVERVIEW P 4

2. CONFIGURATION

2.1. BOOT OPTION P 4
2.2. JTAG INTERFACE P 4
2.3. CLOCK SELECTION P 5

3. COMPONENTS

3.1. SEVEN SEGMENT DISPLAY P 6

1. Introduction

1.1. Block Diagram

Prometheus is an **FPGA**(**F**ield **P**rogrammable **G**ate **A**rray) development board, designed by Onurhan Öztürk and Altynbek Isabekov. Based on Xilinx Spartan3A, Prometheus can handle various fundamental needs with it’s wide range of peripherals.

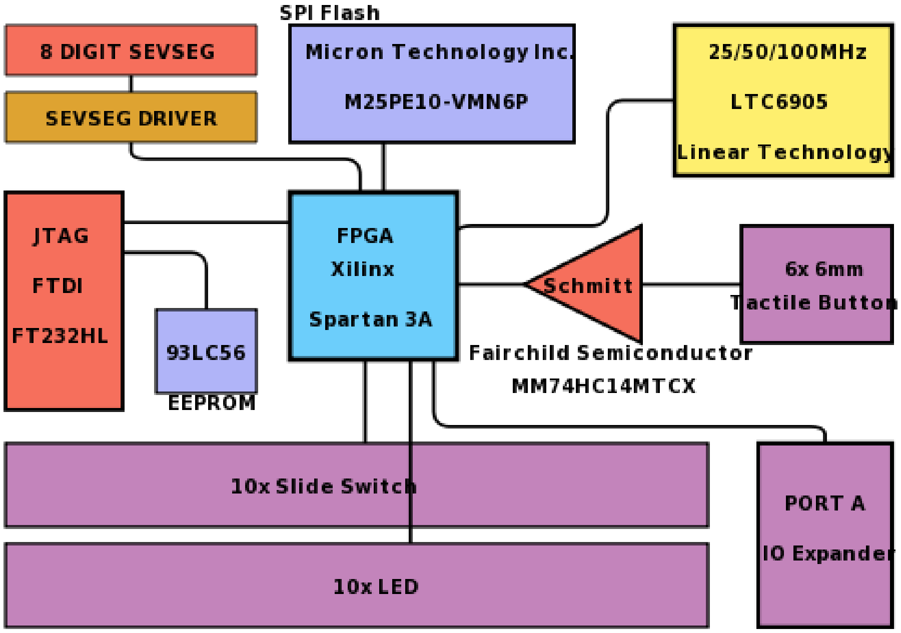


Figure 1: Block Diagram

INPUT

6x Tactile Buttons
25/50/100 MHz Clock

Port A - IO Expander

OUTPUT

10x Slide Switchs
10x LEDs
8 Digit 7SEG
Port A - IO Expander

1.2. Board Overview

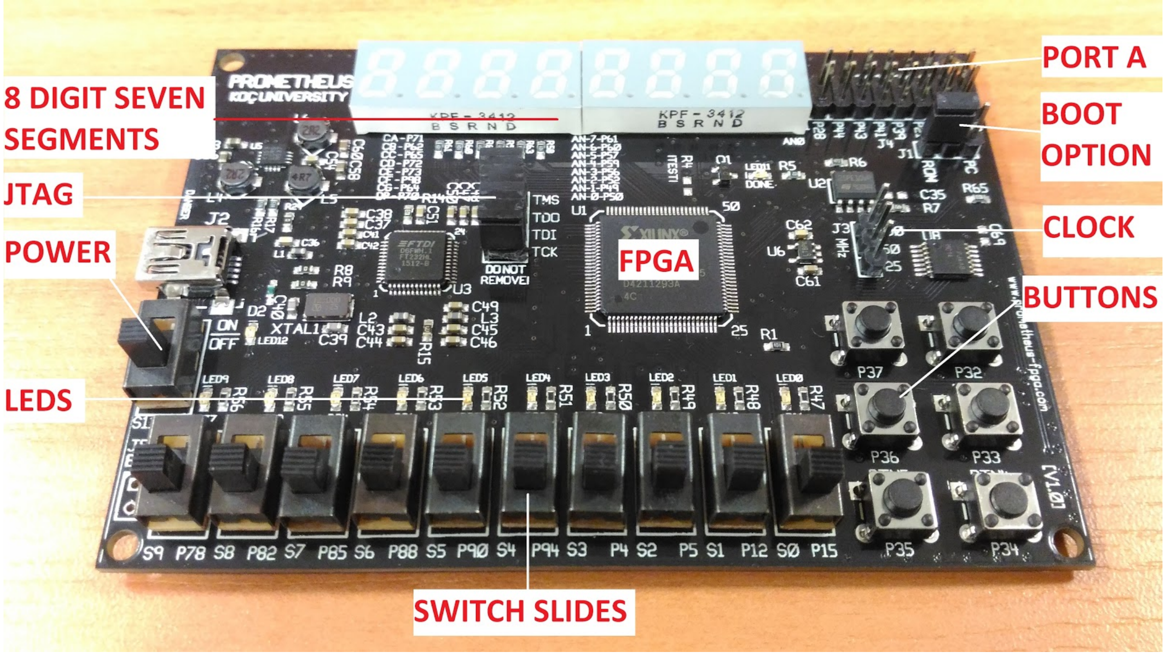


Figure 2: Board Overview

2. Configuration

2.1 BOOT OPTION

When Prometheus is powered up by a USB cable or an external power supply through connector J5, Spartan 3A will boot itself according to value of jumper J1. If jumper is positioned on left, previously stored program on SPI Flash memory will be loaded into FPGA and start running automatically. Else if, FPGA will pull-up all I/O pins to prevent any conflicting configuration and wait for an JTAG instruction.

2.2 JTAG INTERFACE

Keep in mind that **JTAG**(**J**oint **T**est **A**ction **G**roup) is an industry standard protocol developed by IEEE Standard 1149.1-1990, entitled as Standard Test Access Port and Boundary-Scan Architecture. It is the most fundamental and low-level interface for an integrated circuit to debug. This manual will not go deeper in JTAG but for people who are interested about it, we strongly recommend you to read;

https://www.xilinx.com/support/documentation/user_guides/ug332.pdf *(JTAG Configuration Mode and Boundary-Scan, P200)*

Just like most of the other IC's in the market, Spartan 3A has a 4-wire JTAG bus consisting of TMS,TCK,TDO and TDI lines. This bus is driven by a FTDI FT232H chip through USB protocol. Keep in mind that USB is a high level protocol. On the contrary JTAG low level, this data conversion is done by a module called MPSSE. *MPSSE Mode is designed to allow the FT232H to interface efficiently with synchronous serial protocols such as JTAG, I2C and SPI (MASTER) Bus. It can also be used to program SRAM based FPGA's over USB. The MPSSE interface is designed to be flexible so that it can be configured to allow any synchronous serial protocol (industry standard or proprietary) to be implemented using the FT232H.* For detailed information please read;

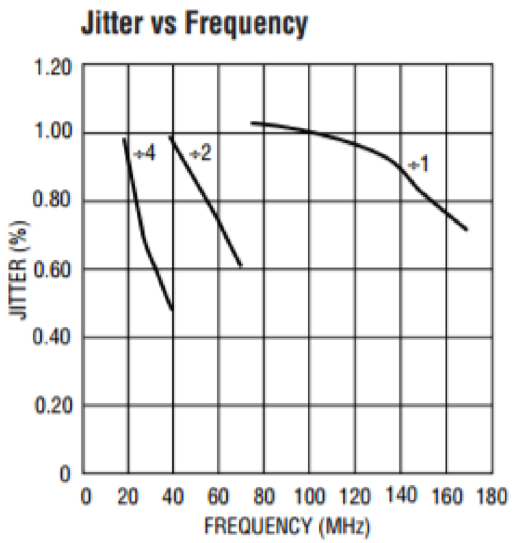
http://www.ftdichip.com/Support/Documents/DataSheets/ICs/DS_FT232H.pdf (*MPSSE Interface Mode Description*, P37)

Due to this generic property of JTAG, you can technically use the JTAG connectors on the board to debug almost all devices, which you have access to JTAG pins. On the other hand, moment you unplug a single jumper on J6, communication between Spartan3A and FireProg will be interrupted and **programming of both FPGA and the Flash Memory will be impossible!**

For stable operation, DO NOT REMOVE any of the jumpers on J6.

2.3 CLOCK SELECTION

Prometheus board is powered by an on-board frequency selectable clock generator to make sequential programming easier and faster! With the help of J3, you can easily feed your program by either 25, 50 or 100MHz with a typical of ∓0.5% frequency error.



For 100MHz,
Set Jumper TOP
For 50MHz
Set Jumper HORIZONTAL
For 25MHz
Set Jumper BOTTOM

Clock Pin of the FPGA : P40

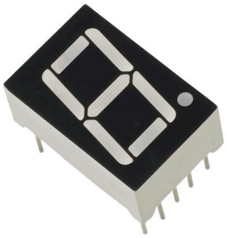
3. COMPONENTS

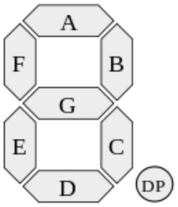
3.1 SEVEN SEGMENT DISPLAY

When it comes to display non-binary data, a set of seven segment digits can be handy. Thankfully, Prometheus consists of 8 Digit 7-Segment displays. In order to display a something that makes, we have to write a simple driver. For people who says “I don’t really care how it works, just tell me how to make it work”, a GNU licensed library **SSSLib** (Simple Seven Segment Library , *written by us*) is provided on www.prometheus-fpga.com. And for people who say “Tell me how to do!” can keep reading…

What is a Seven Segment Display?

A seven segment display is a matrix of leds manufactured in a robotic 8 shape. With the help of parallel pins, it is possible to turn on or off each individual segment to create different symbols. Globally there is a conventional way to define segments with letters. On right you can see an example how each segment is labeled by a letter. (*dot point is a segment but it is counted in 7*)





There are total of 8 of these seven segment digits on-board which are connected in Common Anode configuration. For detailed information please search “common anode vs common cathode”. If we were to connect each segment of each digit to a pin on FPGA, it would require 8 x (7+1) = 64 pins. Unfortunately this is not an optimum solution. To lower the number of required pins, we have implemented a technique called multiplexing. In this technique, each segment is shared among all digits and each digit has a master power pin. That means, if you turn on Segment B and power pins of all digits, all of the B segments will turn on. However, if you were to power only digit 0 and segment A, then digit 1 and segment B with a frequency around 100Hz(f > 30 human eye), your eye would only see segment A lighting on digit 0 and segment B lighting on digit 1. This is the fundamental idea behind driving a seven segment display. By the help of this configuration, we can reduce the required number of pins to #digits + (7+1) = 16!

For a better visualization you can watch https://youtu.be/R9kUadTXpzs?t=2m13s

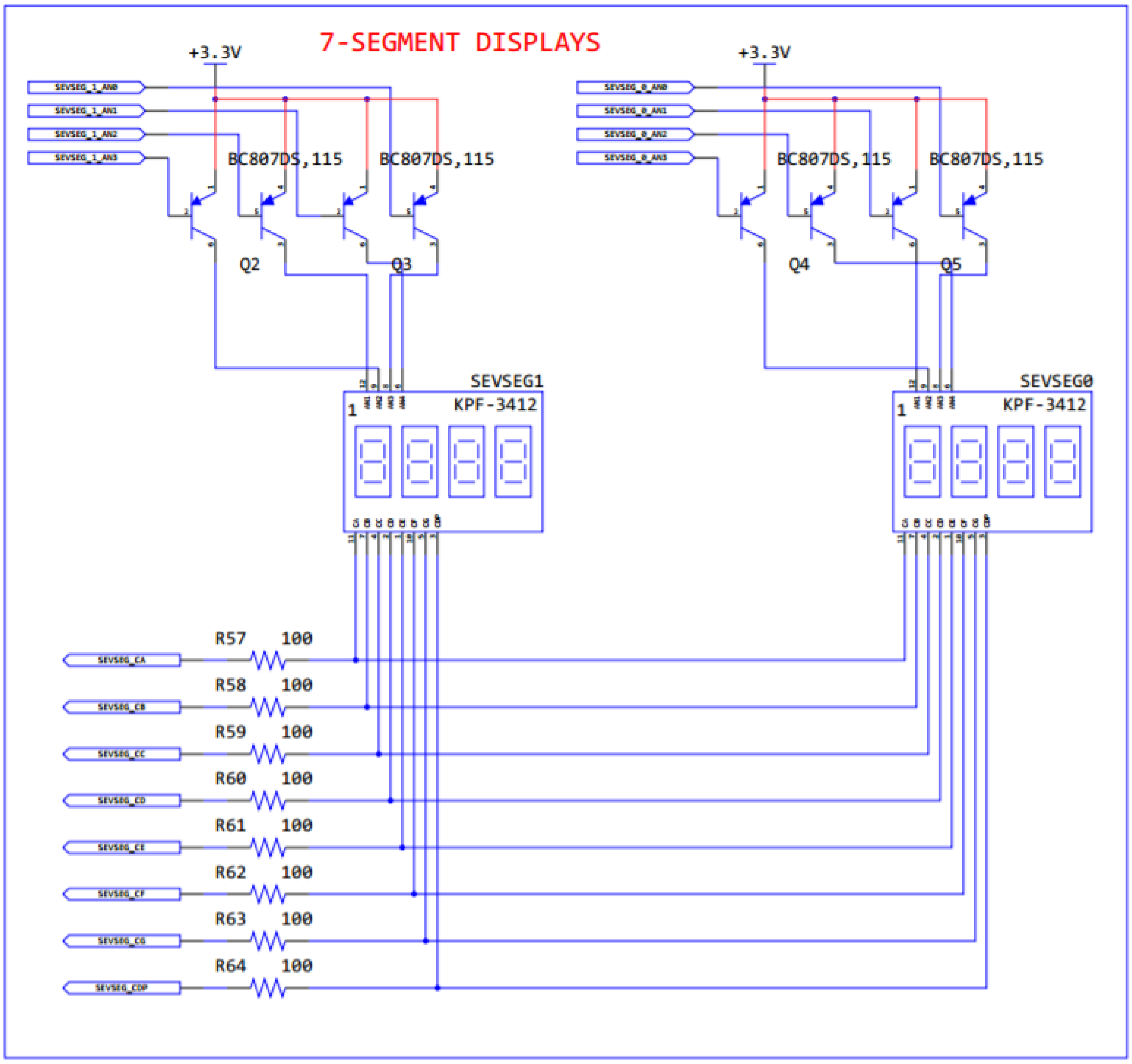


Figure 3: 7-Segment Display from Schematic

Pin MAP to FPGA

ANODES	COMMON SEGMENTS
A0 - P50	CA - P71
A1 - P49	CB - P62
A2 - P52	CC - P65
A3 - P56	CD - P72
A4 - P59	CE - P73
A5 - P57	CF - P98
A6 - P60	CG - P64
A7 - P61	CH - P70

APPENDIX A:

REVISION HISTORY

1. Revision 1.0 (January 2017) This is the initial released version of the document.